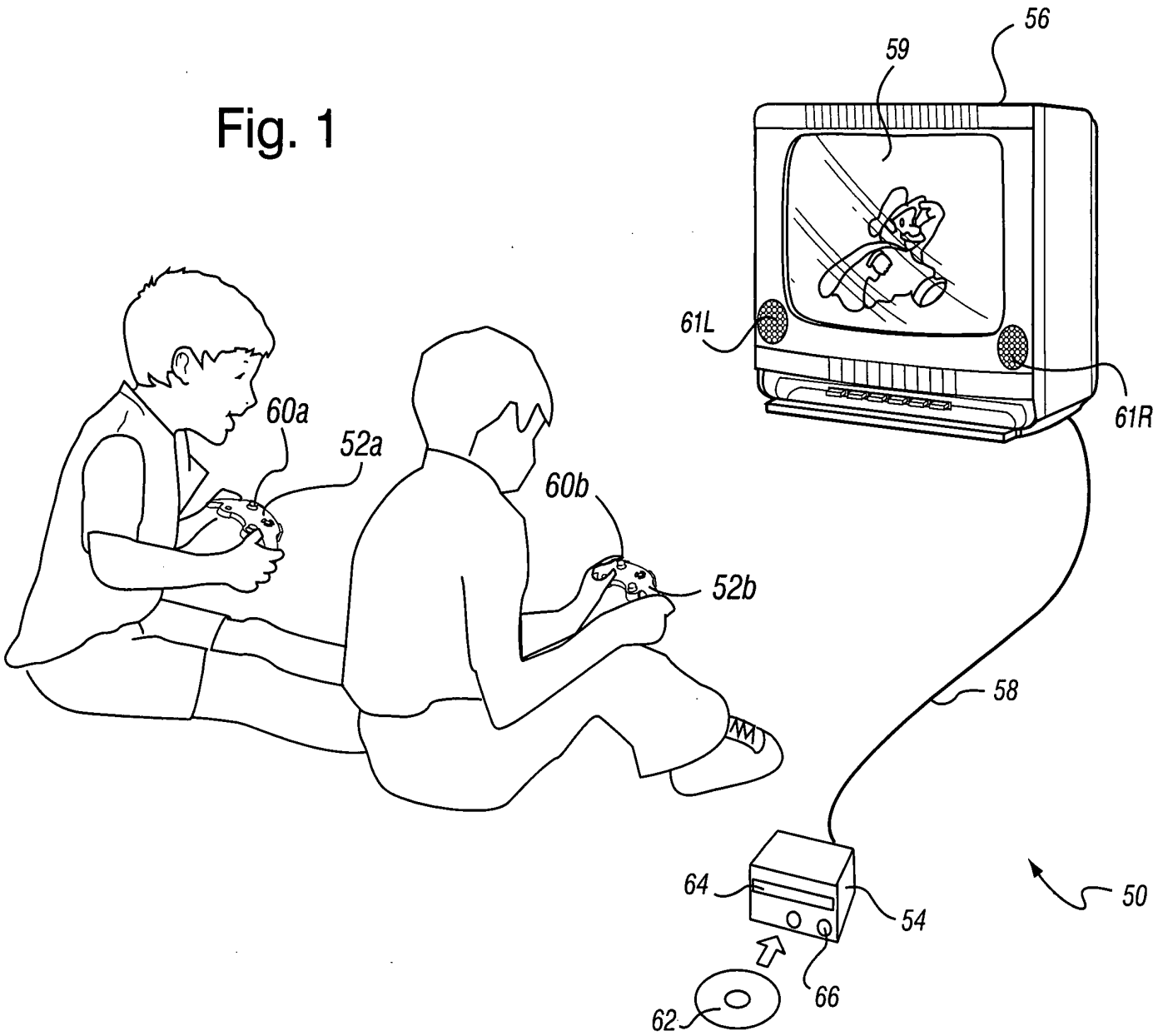
APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS SUBCLASS

Fig. 1



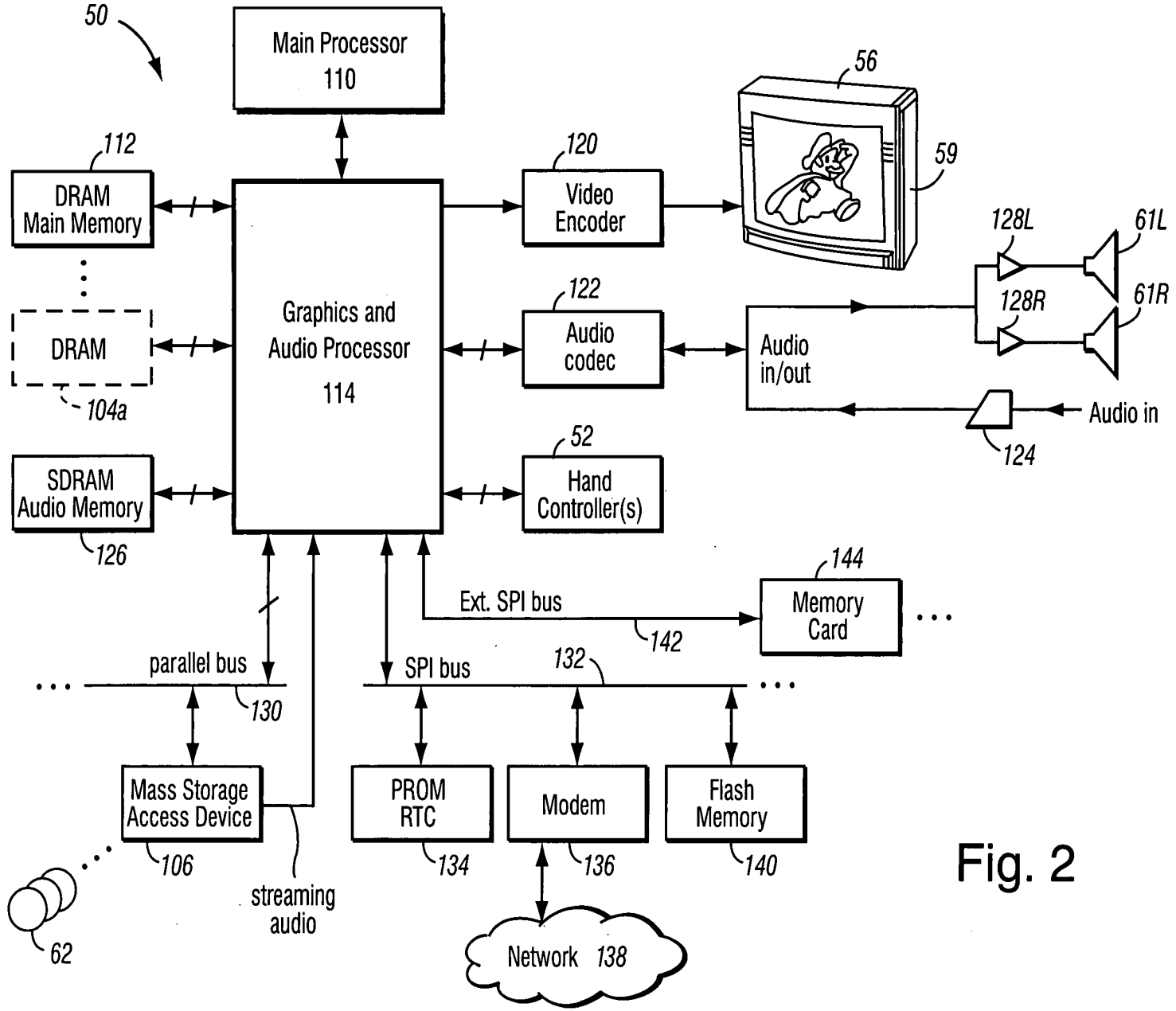

50
Main Processor
110
112
DRAM
Main Memory
DRAM
104a
SDRAM
Audio Memory
126
Graphics and
Audio Processor
114
120
Video
Encoder
56
59
122
Audio
codec
128L
61L
128R
61R
Audio
in/out
Audio in
124
52
Hand
Controller(s)
144
Memory
Card
Ext. SPI bus
142
parallel bus
130
SPI bus
132
Mass Storage
Access Device
106
PROM
RTC
134
Modem
136
Flash
Memory
140
streaming
audio
62
Network 138

Fig. 2

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS

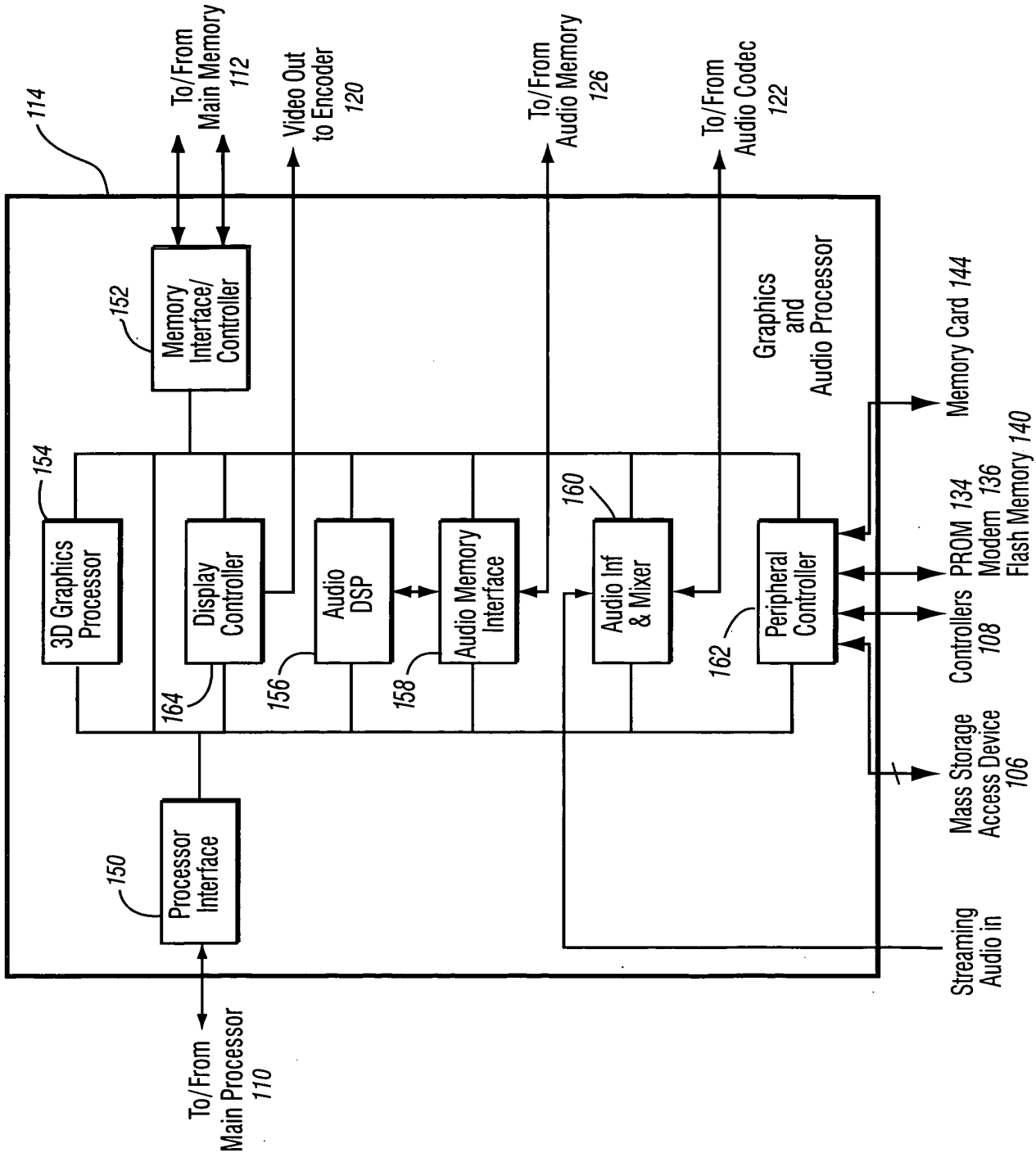


Fig. 3

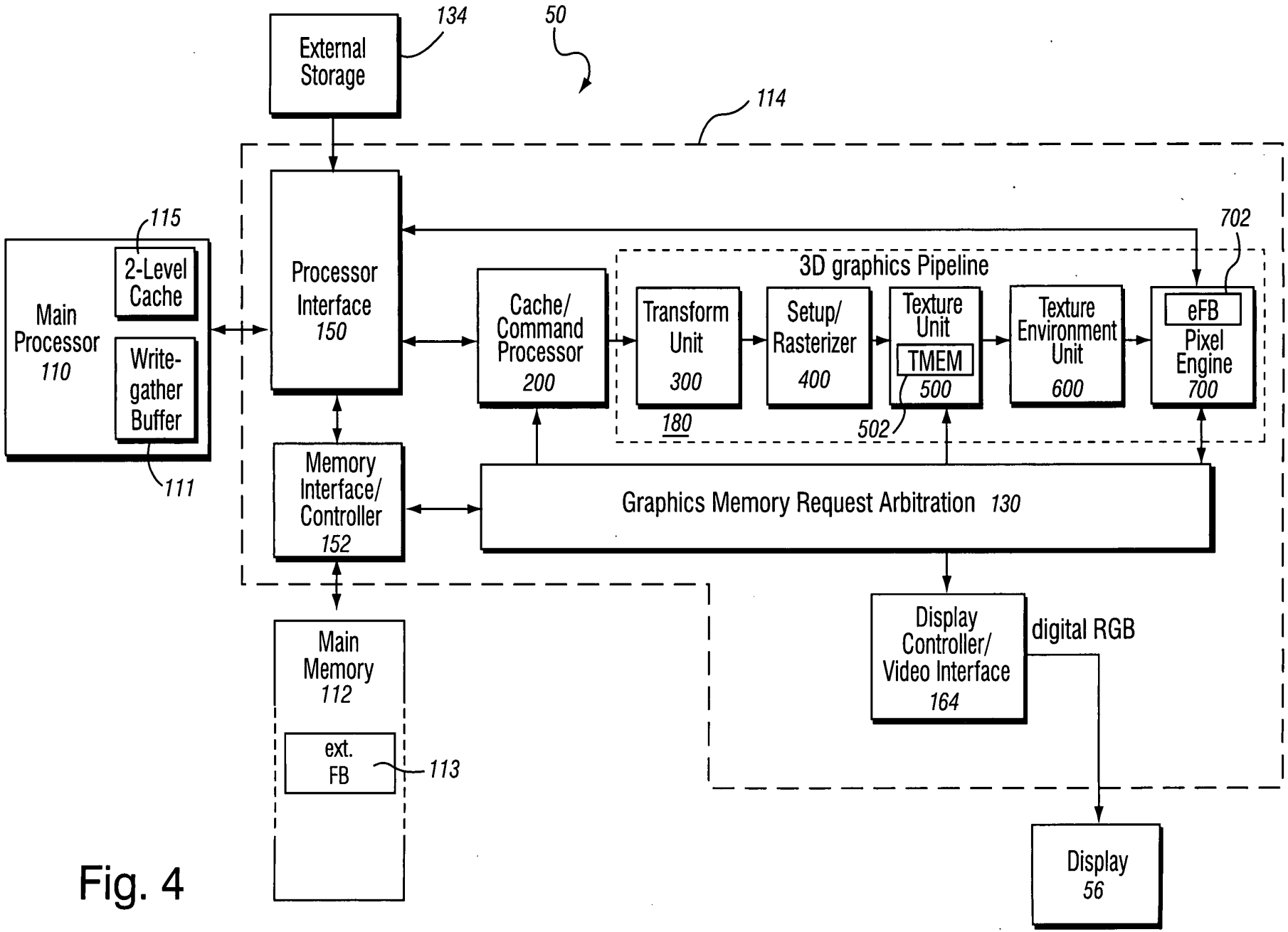

External Storage
134
50
114
115
2-Level Cache
Main Processor 110
Write-gather Buffer
111
Processor Interface 150
Cache/ Command Processor 200
3D graphics Pipeline
Transform Unit 300
Setup/ Rasterizer 400
Texture Unit
TMEM 500
Texture Environment Unit 600
eFB
Pixel Engine 700
702
180
502
Memory Interface/ Controller 152
Graphics Memory Request Arbitration 130
Main Memory 112
ext. FB
113
Display Controller/ Video Interface 164
digital RGB
Display 56

Fig. 4

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS

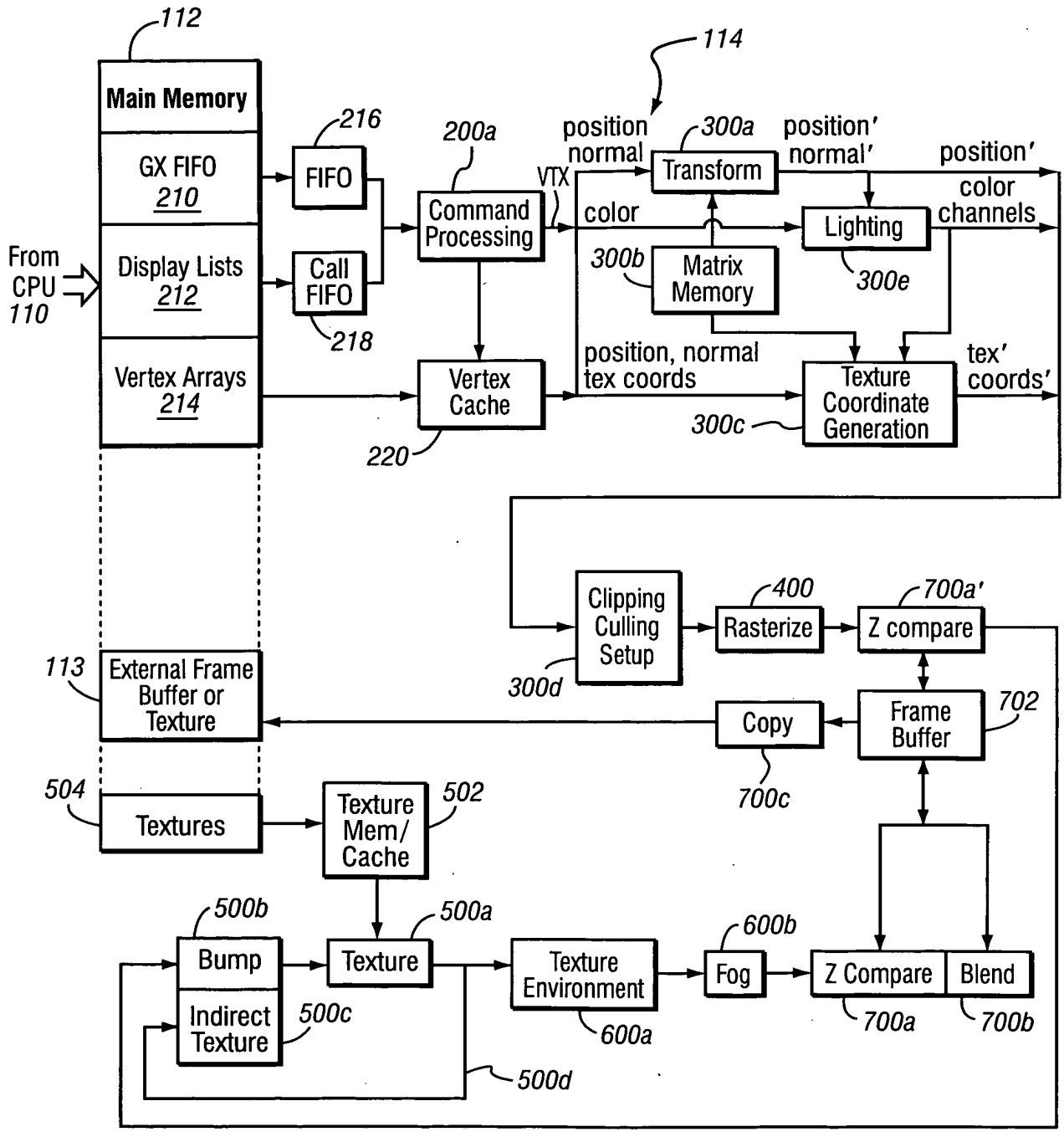
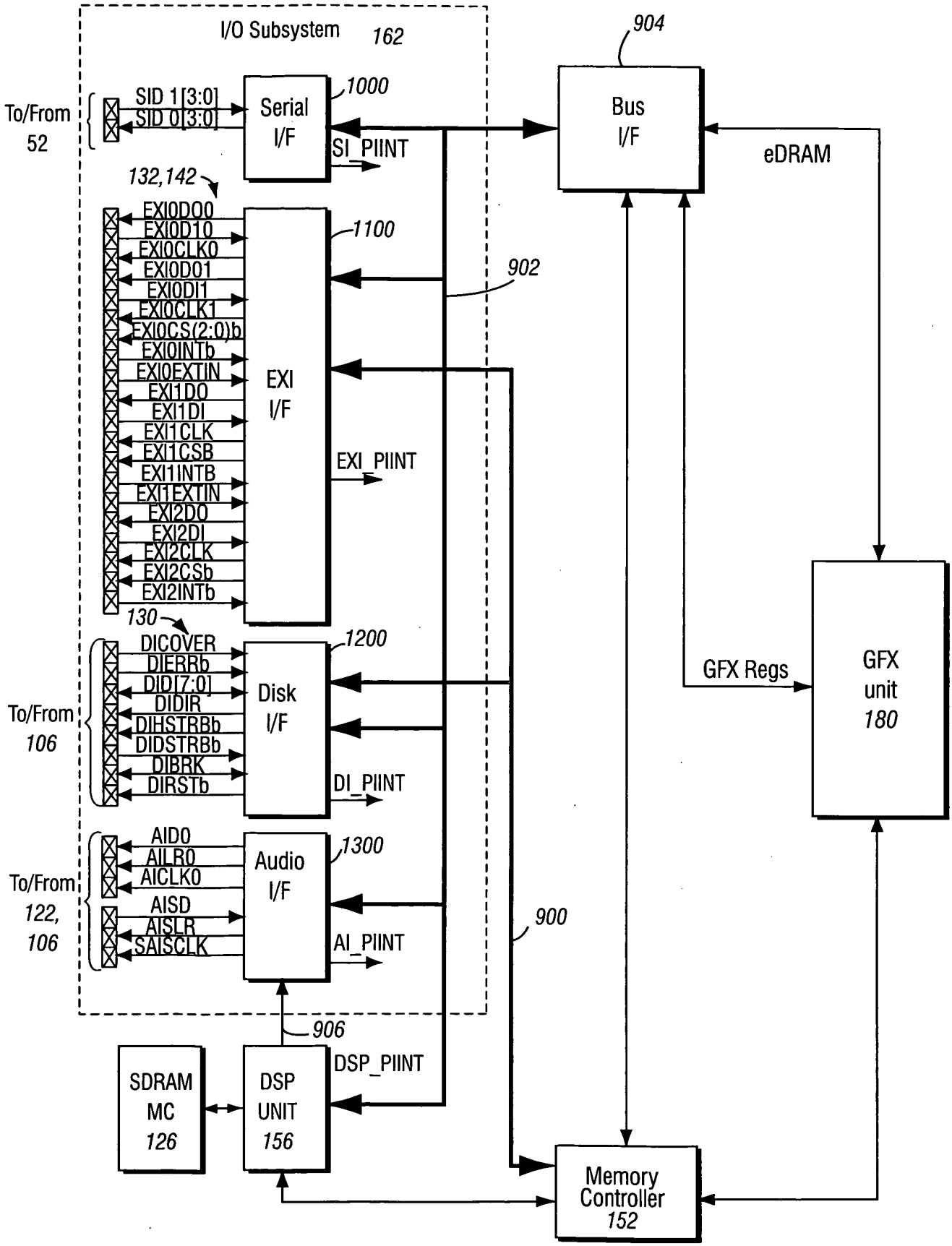


Fig. 5 EXAMPLE GRAPHICS PROCESSOR FLOW

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

Fig. 6 EXAMPLE PERIPHERAL CONTROLLER BLOCK DIAGRAM



APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

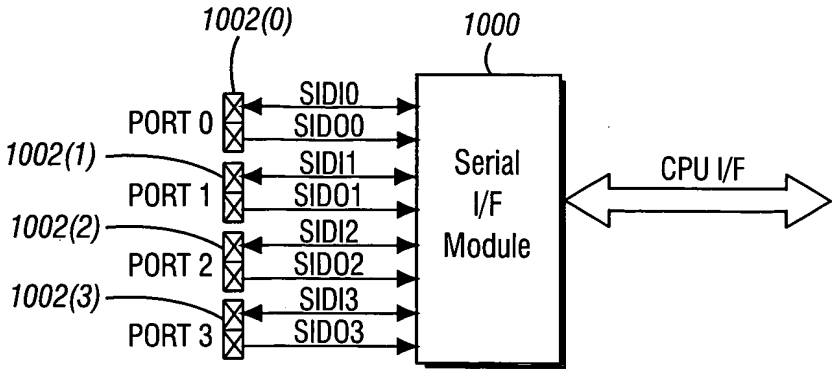


Fig. 7A
EXAMPLE SERIAL INTERFACE

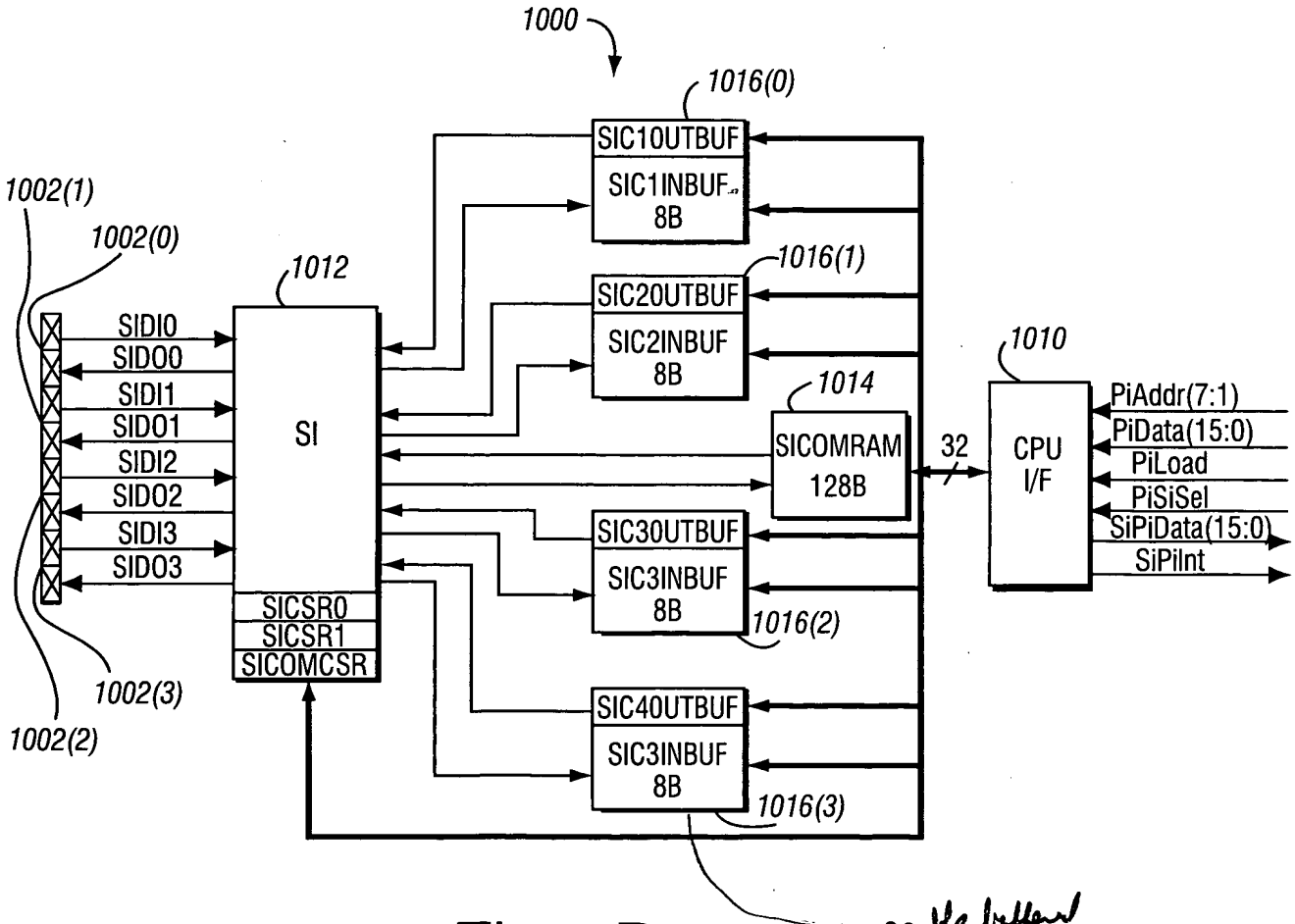


Fig. 7B
EXAMPLE SERIAL INTERFACE

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

Register				Offset(hex)
31	16	15	0	
SI Channel 0 Output Buffer (SIC0OUTBUF)				0x00
SI Channel 0 Input Buffer H (SIC0INBUFH)				0x04
SI Channel 0 Input Buffer L (SIC0INBUFL)				0x08
SI Channel 1 Output Buffer (SIC1OUTBUF)				0x0C
SI Channel 1 Input Buffer H (SIC1INBUFH)				0x10
SI Channel 1 Input Buffer L (SIC1INBUFL)				0x14
SI Channel 2 Output Buffer (SIC2OUTBUF)				0x18
SI Channel 2 Input Buffer H (SIC2INBUFH)				0x1C
SI Channel 2 Input Buffer L (SIC2INBUFL)				0x20
SI Channel 3 Output Buffer (SIC3OUTBUF)				0x24
SI Channel 3 Input Buffer H (SIC3INBUFH)				0x28
SI Channel 3 Input Buffer L (SIC3INBUFL)				0x2C
SI Poll Control Register (SIPOLL)				0x30
SI Communication Control Status Register (SICOMCSR)				0x34
SI Status Register (SISR)				0x38
SI EXI Lock Register (SIEXILK)				0x3C
SI Communication RAM (128 Bytes)				0x80-0xFF

Fig. 7C

EXAMPLE SERIAL INTERFACE REGISTERS

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

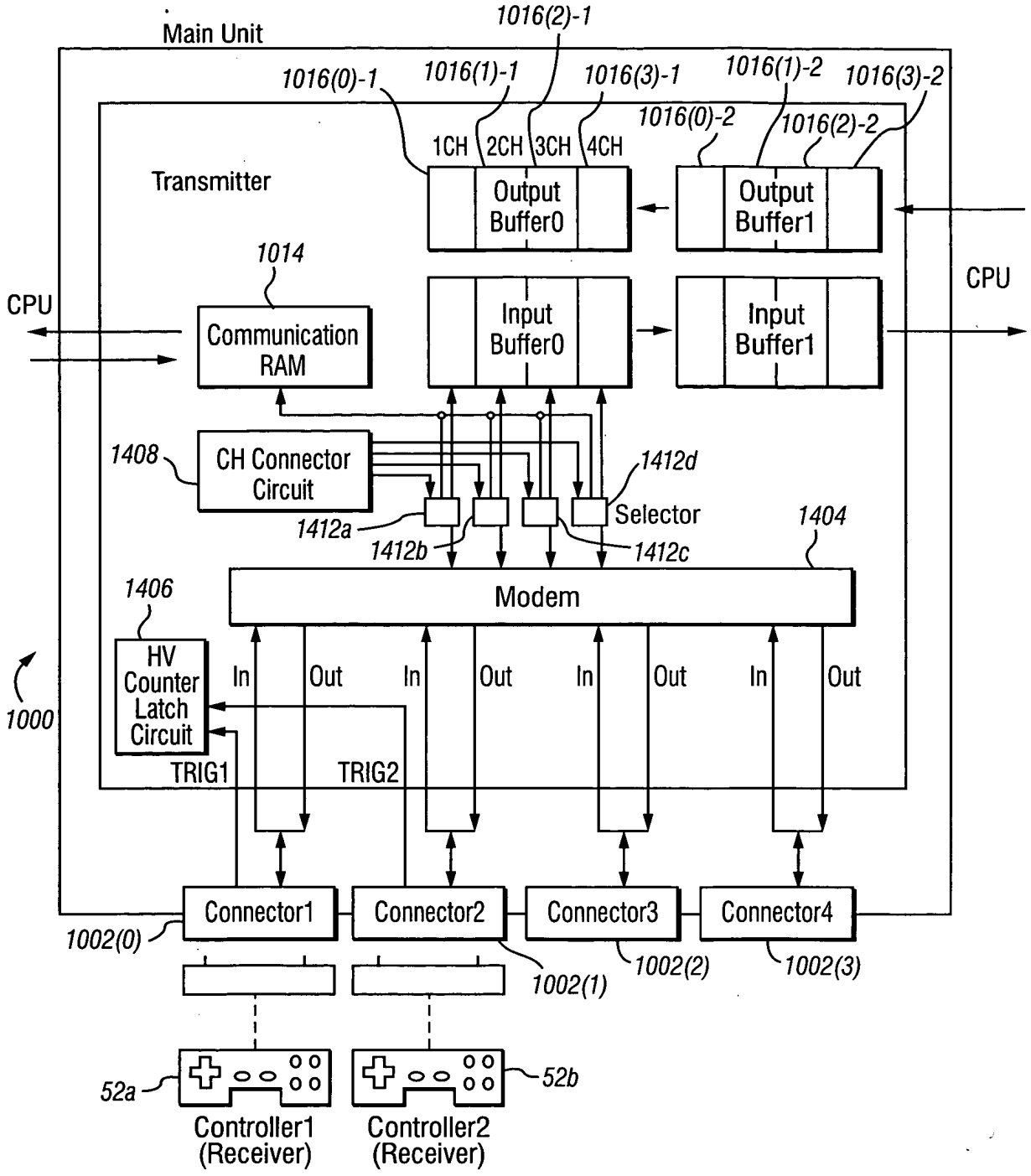


Fig. 8

EXAMPLE SERIAL INTERFACE

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

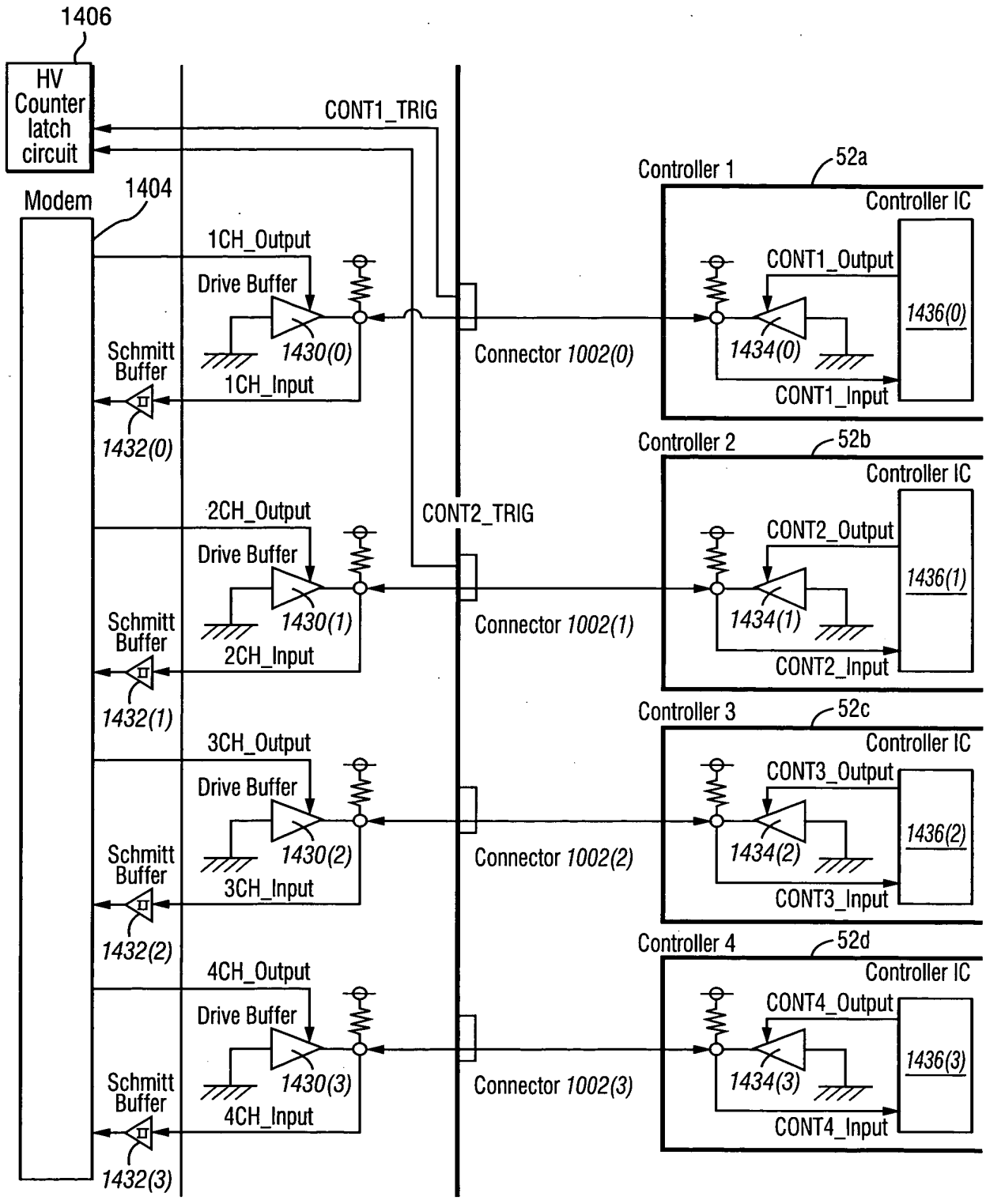


Fig. 9

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

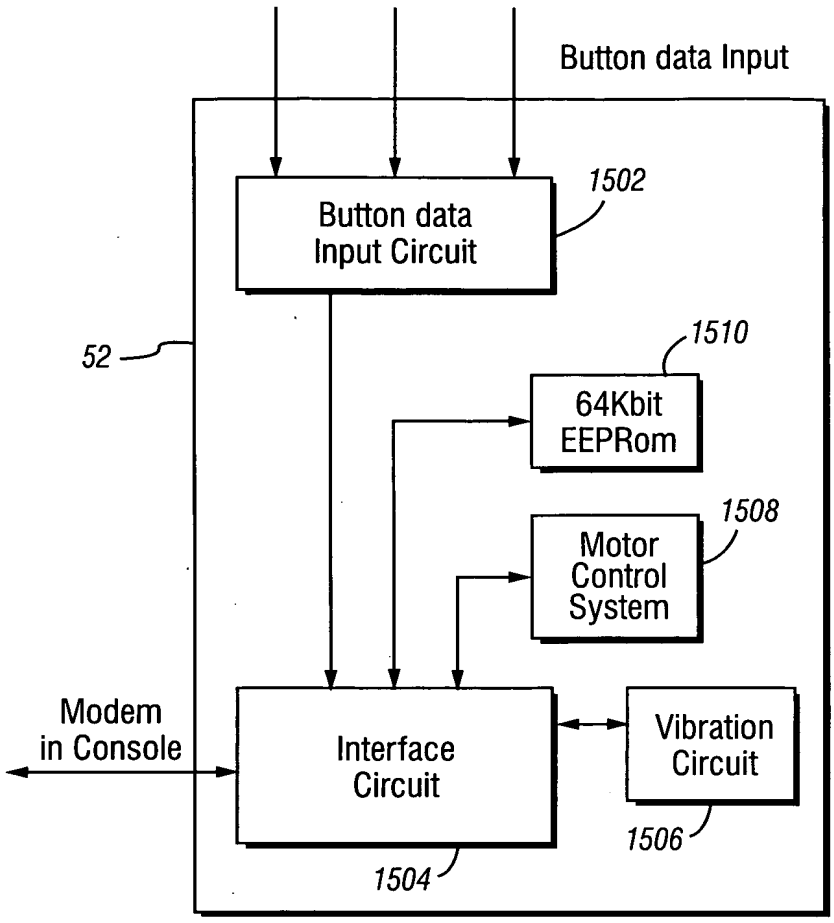


Fig. 10

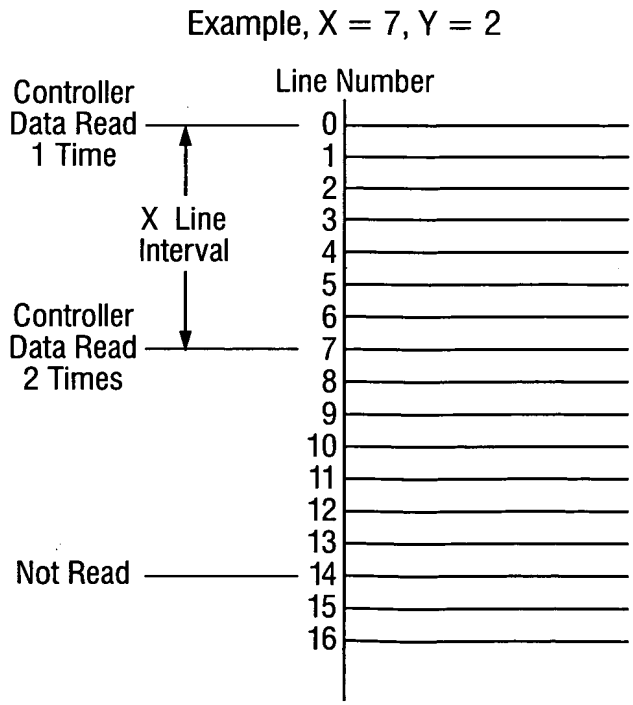


Fig. 12

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

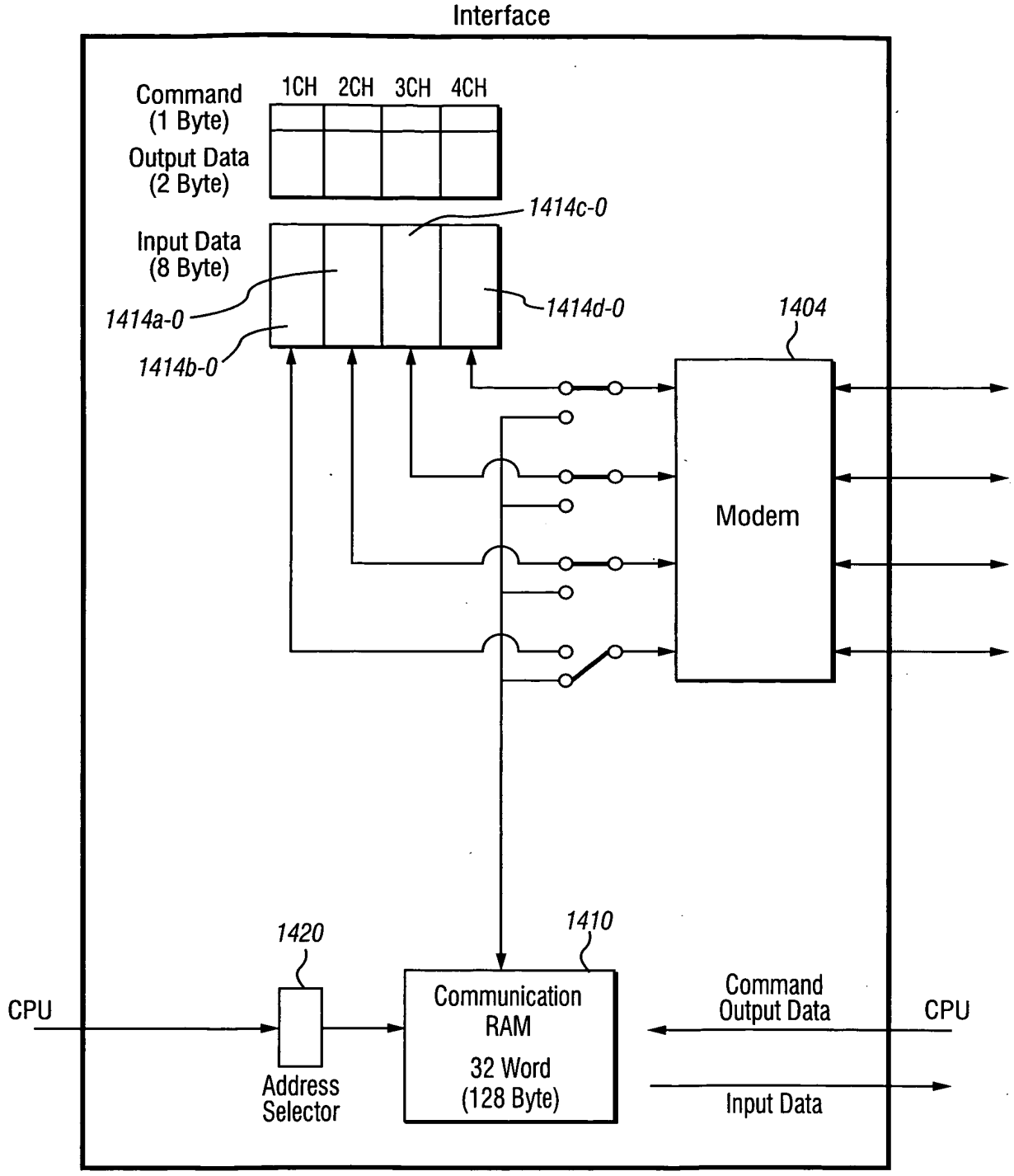


Fig. 11

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

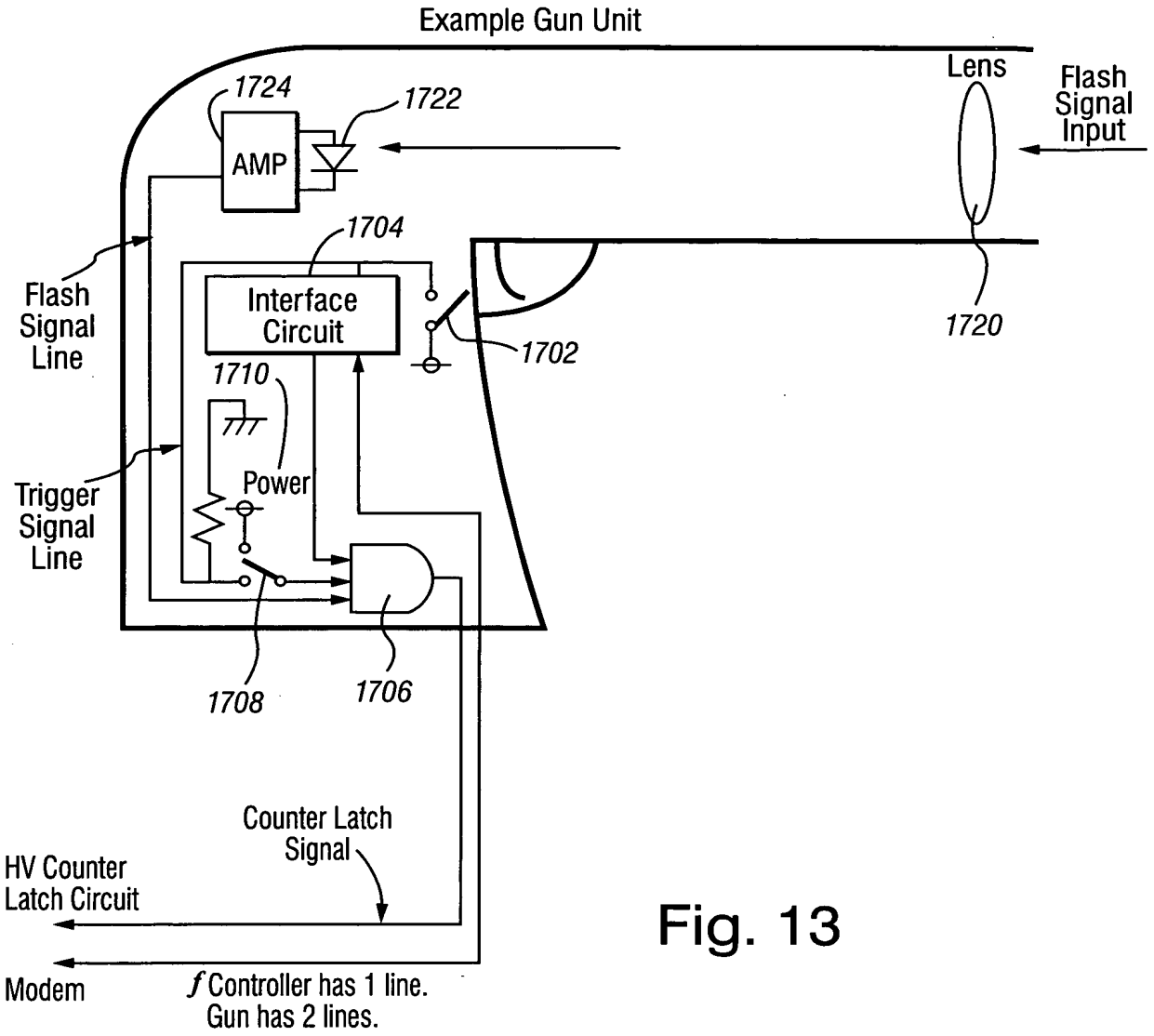


Fig. 13

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

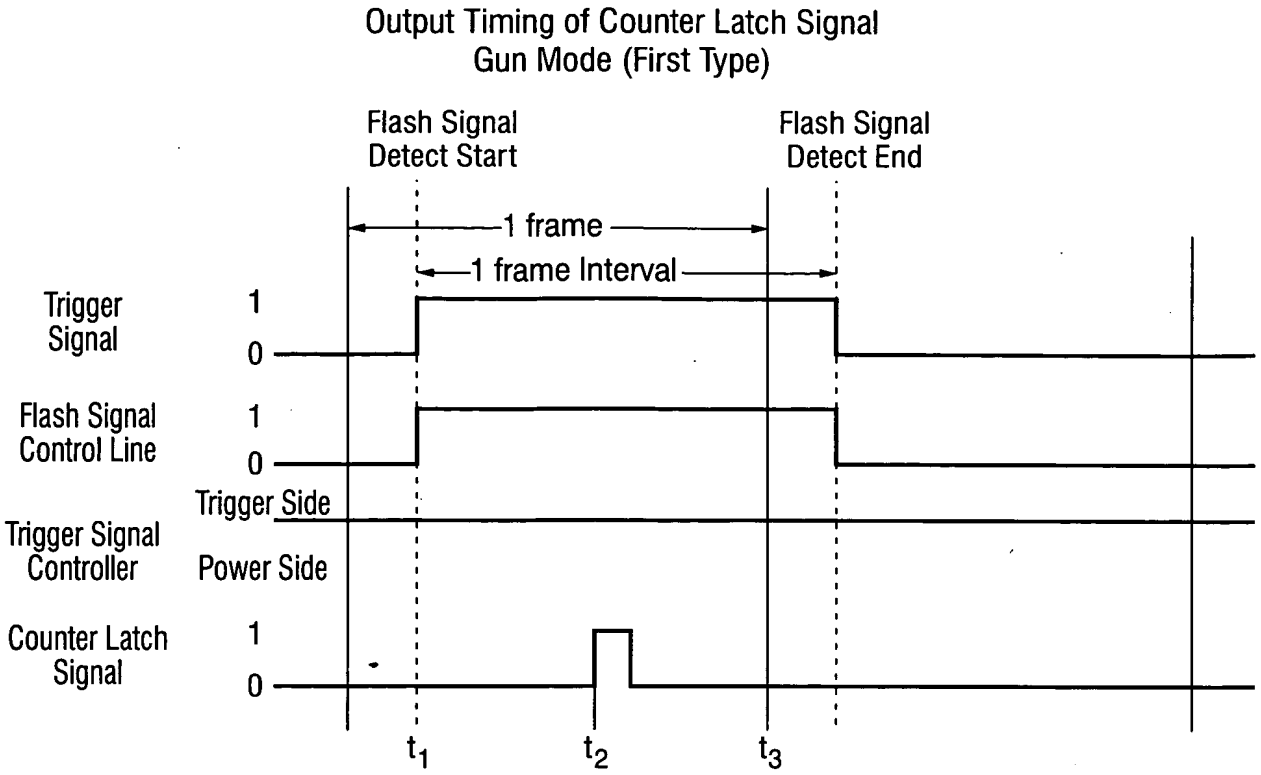


Fig. 14A

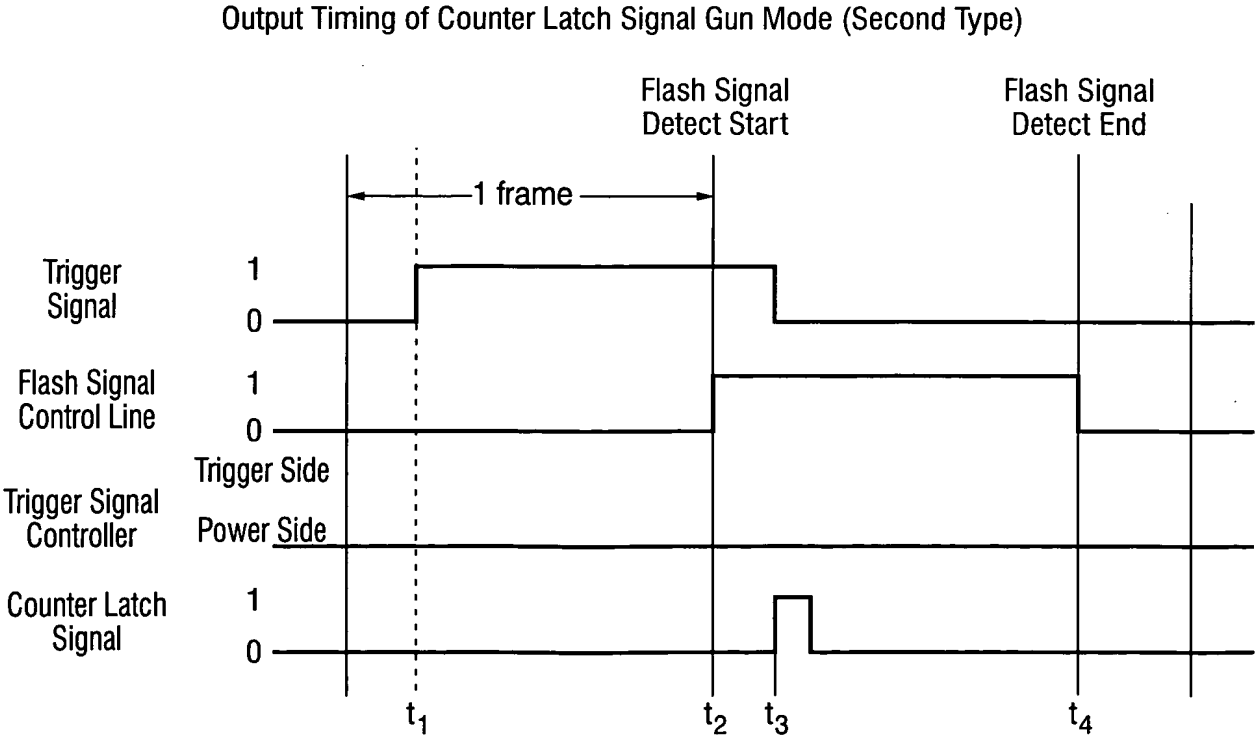


Fig. 14B

APPROVED BY DRAFTSMAN | O.G. FIG. | CLASS | SUBCLASS

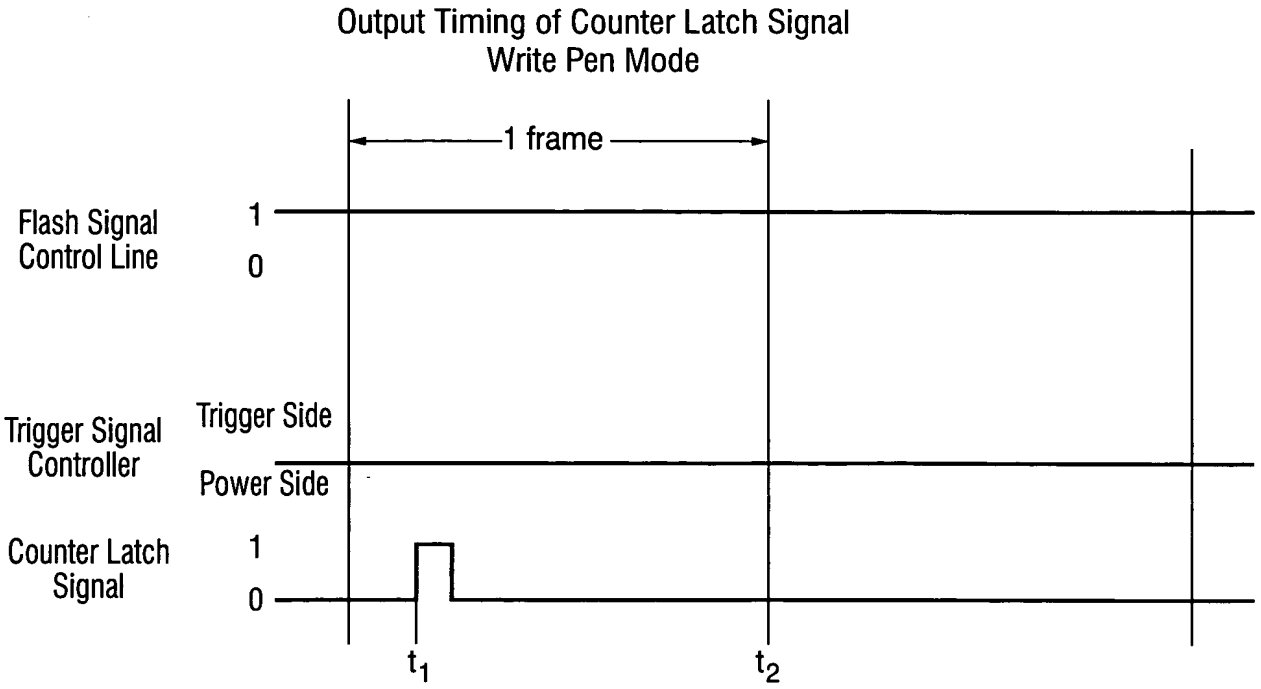


Fig. 14C

O.G. FIG.
BY | CLASS | SUBCLASS
DRAFTSMAN

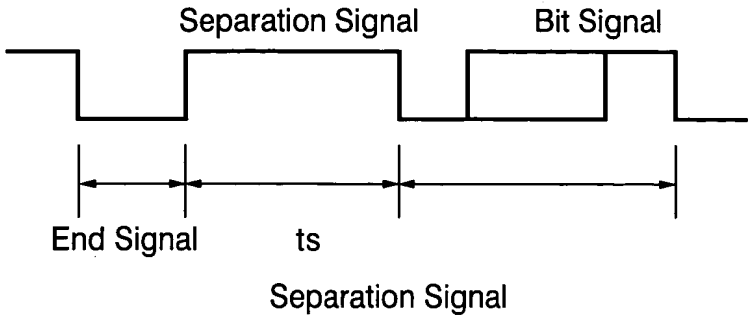


Fig. 15A

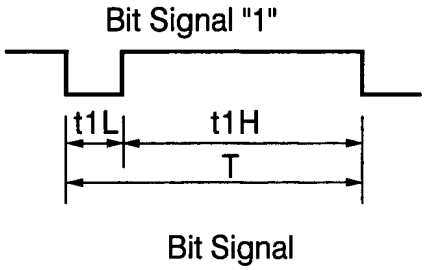


Fig. 15B

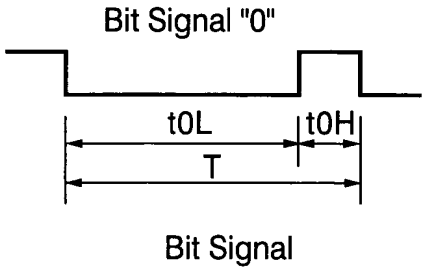


Fig. 15C

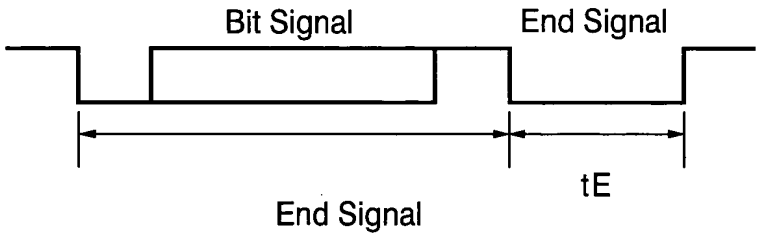


Fig. 15D

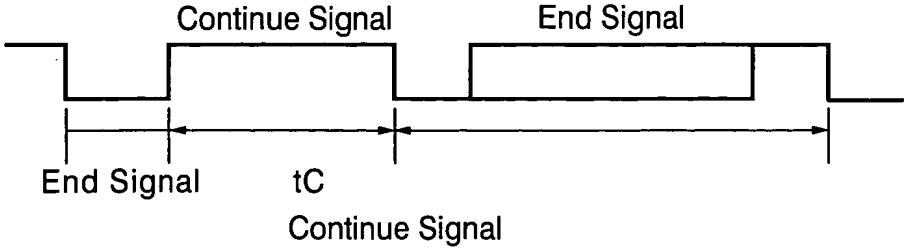
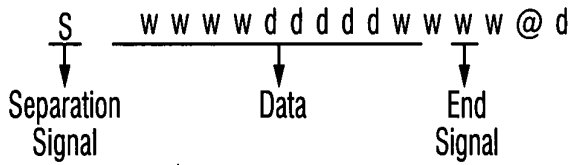


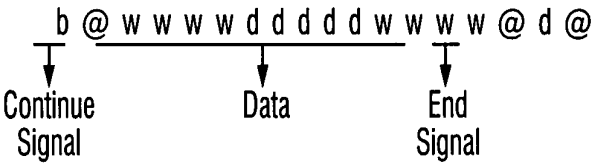
Fig. 15E

BY
CRAFTSMAN
CLASS
SUBCLASS
O.G. FIG.



Command Frame

Fig. 16A



Response Frame

Fig. 16B

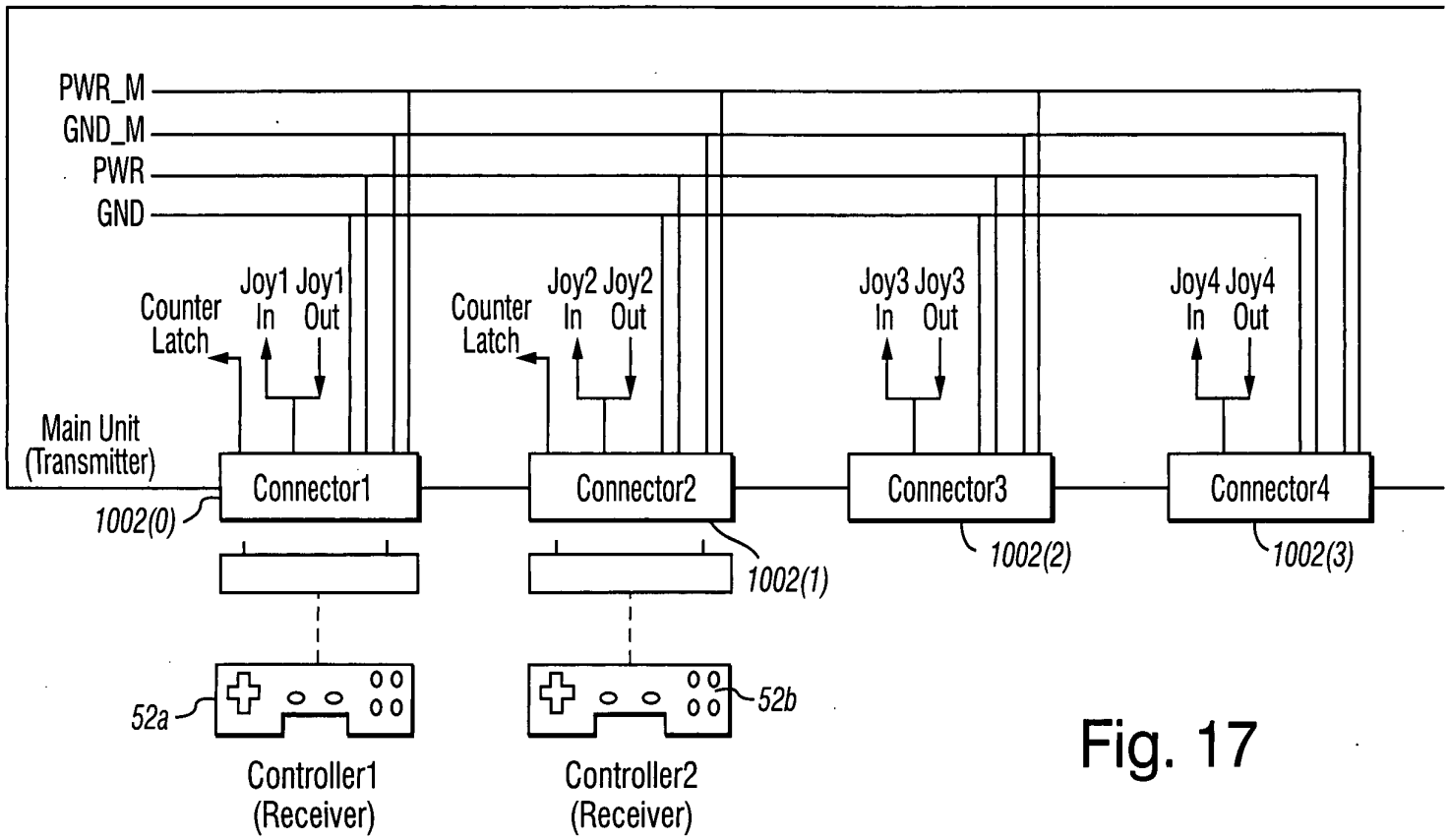


Fig. 17

APPROVED
BY
DRAFTSMAN
O.G. FIG.
CLASS
SUBCLASS

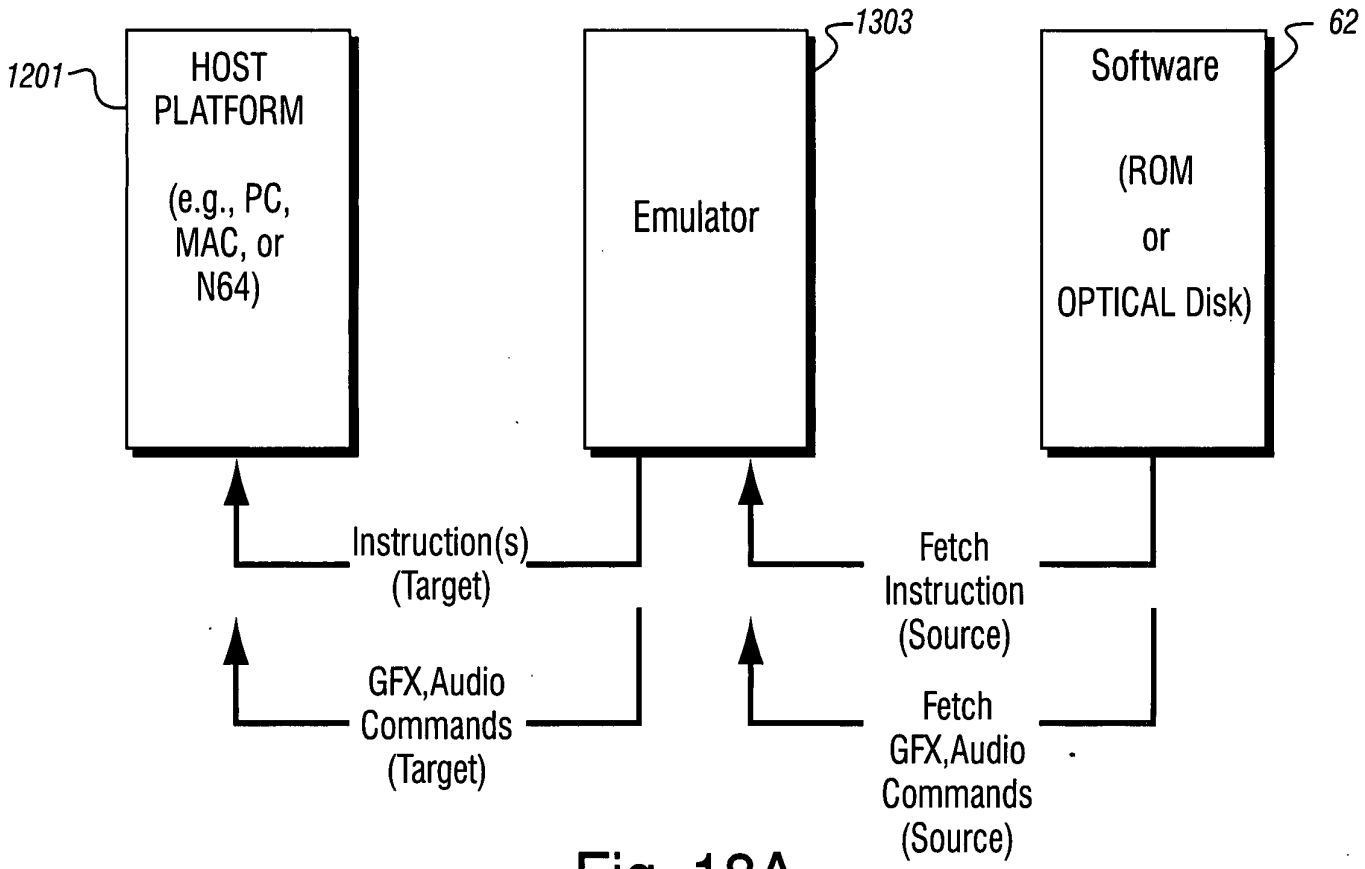


Fig. 18A

APPROVED BY DRAFTSMAN
O.G. FIG.
CLASS SUBCLASS

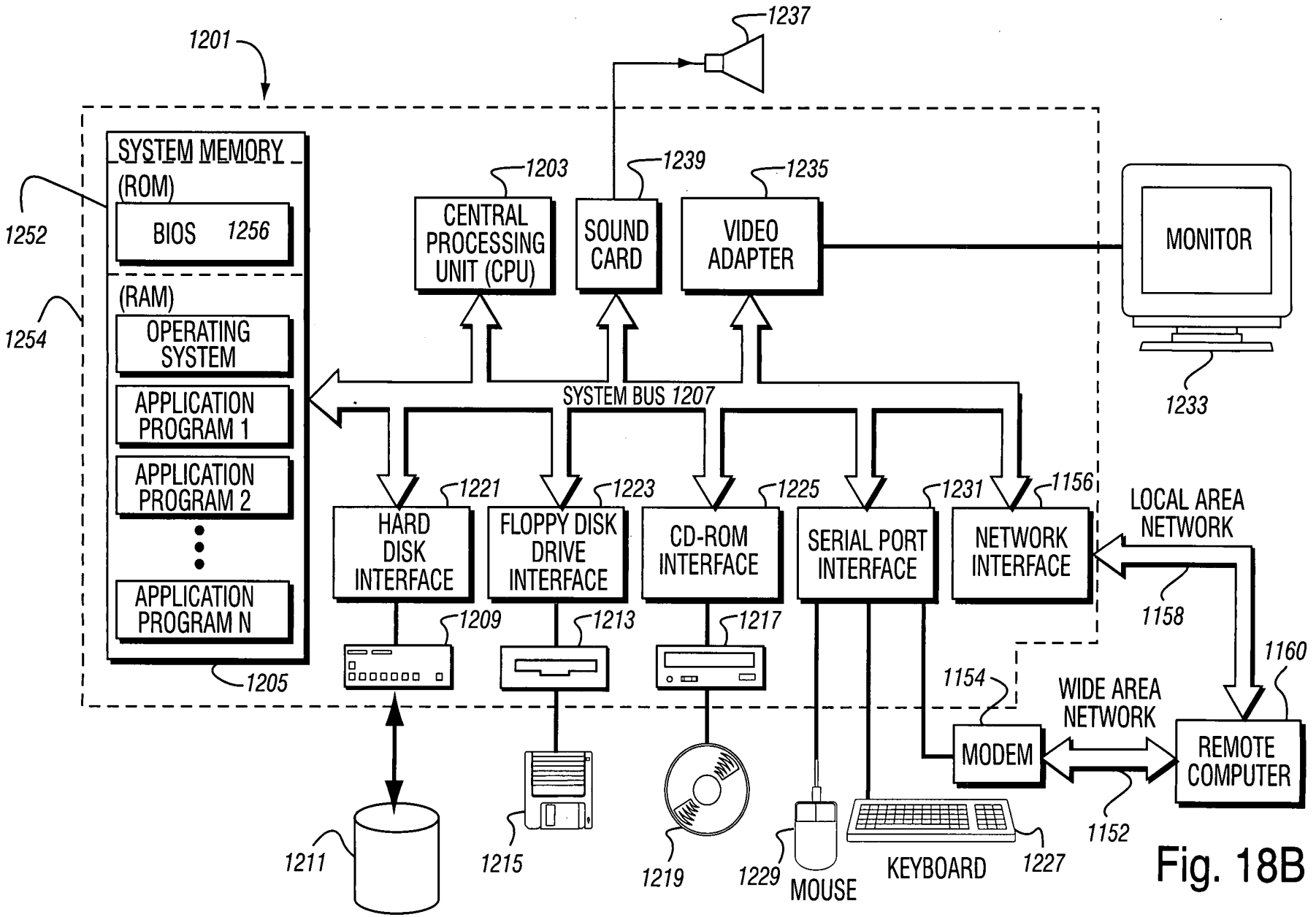


Fig. 18B